LM3242

6MHz, 750mA Miniature, Adjustable, Step-Down DC-DC Converter with Auto Bypass for RF Power Amplifiers

General Description

The LM3242 is a DC-DC converter optimized for powering RF power amplifiers (PAs) from a single Lithium-Ion cell; however, it may be used in many other applications. It steps down an input voltage from 2.7V to 5.5V to an adjustable output voltage from 0.4V to 3.6V. Output voltage is set using a VCON analog input for controlling power levels and efficiency of the RF PA.

The LM3242 offers five modes of operation. In PWM mode the device operates at a fixed frequency of 6MHz (typ.) which minimizes RF interference when driving medium-to-heavy loads. At light load, the device enters into ECO mode automatically and operates with reduced switching frequency. In ECO mode, the quiescent current is reduced and extends the battery life. Shutdown mode turns the device off and reduces battery consumption to 0.1 µA (typ.). In low-battery condition Bypass mode reduces the voltage dropout to less than 50 mV (typ.). The part also features a Sleep mode.

The LM3242 is available in a 9-bump lead-free micro SMD package. A high switching frequency (6MHz) allows use of only three tiny surface-mount components: one inductor and two ceramic capacitors.

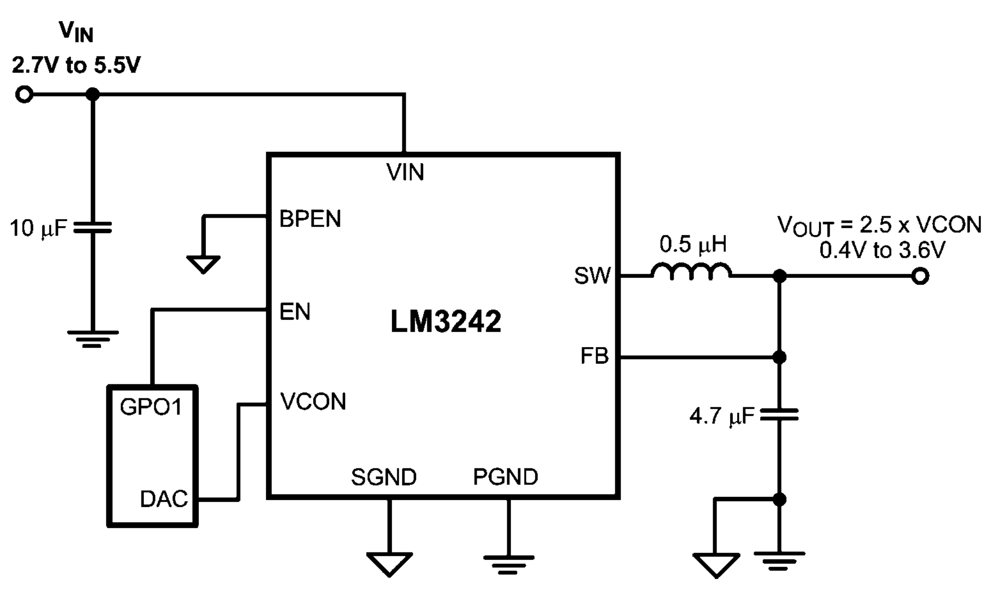
Features

- 6MHz (typ.) PWM Switching Frequency
- Operates from a Single Li-Ion Cell (2.7V to 5.5V)
- Adjustable Output Voltage (0.4V to 3.6V)
- 750 mA Maximum Load Capability (up to 1A in Bypass)
- High Efficiency (95% typ. at $3.9V_{IN}$, $3.3V_{OUT}$ at 500 mA)
- Automatic ECO/PWM/BP mode change
- 9-bump micro SMD Package
- Current Overload Protection
- Thermal Overload Protection
- Soft-Start Function
- Small Chip Inductor in 0805 (2012) case size

Applications

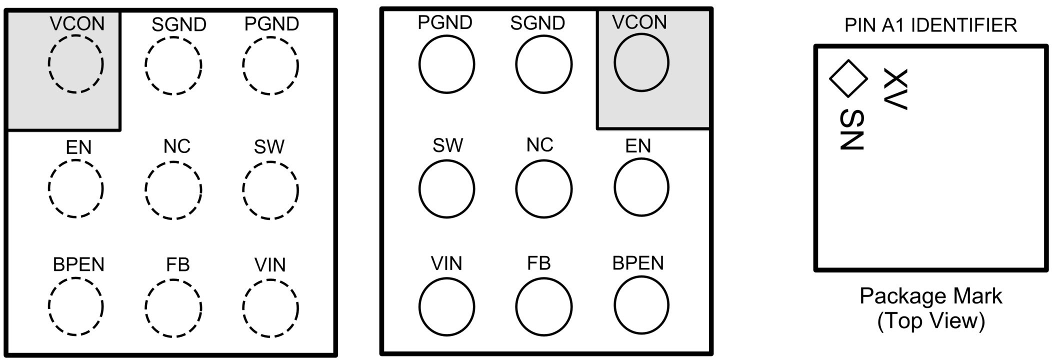
- Battery-Powered 3G/4G RF PAs
- Hand-Held Radios
- RF PC Cards
- Battery-Powered RF Devices

Typical Application



Connection Diagrams and Package Mark Information

9-Bump Thin Micro SMD Package, Large Bump (0.4 mm Pitch)
NS Package Number TMD09



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Note: The actual physical placement of the package marking will vary from part to part. The package marking “XV” designates an internal code for die traceability. “SN” identifies the device (part number, option, etc.).

Order Information

Order Number	Package Marking	Supplied As
LM3242TME	SN	250 units, Tape-and-Reel
LM3242TMX	SN	3000 units, Tape-and-Reel

Pin Descriptions

Pin #	Name	Description
A1	VCON	Voltage Control Analog input. VCON controls V_{OUT} in PWM and ECO modes. VCON may also be used to force bypass condition by setting VCON > V_{IN}/2.5.
A2	SGND	Signal ground for analog and control circuitry.
A3	PGND	Power ground for the Power MOSFETs and gate drive circuitry
B1	EN	Enable Input. Set this digital input high for normal operation. For shutdown, set low. Do not leave EN pin floating.
B2	NC	Do not connect to PGND directly — Internally connected to SGND.
B3	SW	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit specification of the LM3242.
C1	BPEN	Bypass Enable input. Set this digital input high to force bypass operation. For normal operation with automatic bypass, set low or connect to ground. Do not leave this pin floating.
C2	FB	Feedback Analog Input and Bypass FET output. Connect to the output at the output filter capacitor.
C3	VIN	Voltage supply input for SMPS converter.

Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

VIN to SGND	–0.2V to +6.0V
PGND to SGND	–0.2V to +0.2V
EN, VCON, BPEN	(SGND–0.2V) to (VIN+0.2V) w/ 6.0V
SW, FB	(PGND–0.2V) to (VIN+0.2V)
Continuous Power Dissipation (Note 3)	Internally Limited
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	–65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec)	+260°C
ESD Rating (Note 4)	
Human Body Model:	2kV
Machine Model:	200V
Charged Device Model:	1250V

Operating Ratings (Note 1, Note 2)

Input Voltage Range	2.7V to 5.5V
Recommended Load Current	0mA to 750 mA
PWM Mode	0mA to 750 mA
Bypass Mode	0mA to 1000 mA
Junction Temperature (T_J) Range	–30°C to +125°C
Ambient Temperature (T_A) Range (Note 5)	–30°C to +90°C

Thermal Properties

Junction-to-Ambient Thermal Resistance ($θ_{JA}$), TMD09 Package (Note 6)	85°C/W

Electrical Characteristics (Note 2, Note 7, Note 8)

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($–30°C \le T_A = T_J \le +90°C$). Unless otherwise noted, all specifications apply to the Typical Application Circuit (page 1) with VIN = EN = 3.6V, and BPEN = NC = 0V.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{FB,MIN}$	Feedback voltage at minimum setting	PWM mode, VCON = 0.16V (Note 16)	**0.38**	0.4	**0.42**	V
$V_{FB,MAX}$	Feedback voltage at maximum setting	PWM mode, VCON = 1.44V, V_{IN} = 4.0V	**3.55**	3.6	**3.65**	V
I_{SHDN}	Shutdown supply current	EN = SW = VCON = FB = BPEN = NC = 0V (Note 9)		0.1	**1.0**	µA
I_Q_PWM	PWM mode quiescent current	PWM mode, No switching VCON = 0.13V, FB = 1V (Note 10)		650	**795**	µA
I_Q_SLEEP	Low-power SLEEP mode	EN = VIN, BPEN = NC = 0V, SW = TriState VCON < 0.08V (Note 17)		60	**80**	µA
I_Q_ECO	ECO mode Quiescent current	ECO mode, No switching VCON = 0.8V, FB = 2.05V (Note 10)		60	**80**	µA
$R_{DSON (P)}$	Pin-pin resistance for PFET	$V_{IN} = V_{GS}$ = 3.6V, I_{SW} = 200 mA		170	**260**	mΩ
$R_{DSON (N)}$	Pin-pin resistance for NFET	VIN = V_{GS} = 3.6V, I_{SW} = –200 mA		110	**200**	mΩ
$R_{DSON (BP)}$	Pin-Pin resistance for BPFET	$V_{IN} = V_{GS}$ = 3.1V, I_{SW} = –200 mA		80	**110**	mΩ
$I_{LIM P}$	PFET switch peak current limit	(Note 11)	**1300**	1450	**1600**	mA

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{LIM\ BP}$	BPFET switch peak current limit	$V_{FB} = V_{IN} – 1V$ (Note 11)	**310**	400		mA
F_{OSC}	Internal oscillator frequency		**5.7**	6	**6.3**	MHz
V_{IH}	EN, BPEN Logic high input threshold		**1.2**			V
V_{IL}	EN, BPEN Logic low input threshold				**0.4**	V
Gain	VCON to V_{OUT} gain	0.16V ≤ VCON ≤ 1.44V (Note 18)		2.5		V/V
I_{VCON}	VCON pin leakage current	VCON = 1.0V			**±1**	µA
$V_{BP,NEG}$	Auto Bypass Detection Negative Threshold	VCON = 1.2V ($V_{OUT-SET}$ = 3.0V) V_{IN} = 3.2V, R_L = 6Ω (I_{OUT} = 500 mA) (Note 12)	**165**	200	**235**	mV
$V_{BP,POS}$	Auto Bypass Detection Positive Threshold	VCON = 1.2V ($V_{OUT-SET}$ = 3.0V) V_{IN} = 3.25V, R_L = 6Ω (I_{OUT} = 500 mA) (Note 13)	**215**	250	**285**	
$I_{BP,SLEW}$	Auto Bypass I_{OUT} Slew Current	BPEN = High, Forced Bypass		1600		mA

System Characteristics

The following spec table entries are guaranteed by design providing the component values in the Typical Application Circuit are used. **These parameters are not guaranteed by production testing.** Min and Max values apply over the full operating ambient temperature range (–30°C ≤ T_A ≤ 90°C) and over the VIN range = 2.7V to 5.5V unless otherwise specified. L = 0.5 µH, DCR = 50 mΩ, C_{IN} = 10 µF, 6.3V, 0603(1608), C_{OUT} = 4.7 µF, 6.3V, 0402.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{VCON_TR}	V_{OUT} rise time VCON change to 90%	V_{IN} = 3.7V, V_{OUT} = 1.4V to 3.4V 0.1 µs < VCON_T_R < 1 µs, R_L = 12Ω		9		µs
	V_{OUT} fall time VCON change to 10%	V_{IN} = 3.7V, V_{OUT} = 3.4V to 1.4V 0.1 µs < VCON_T_F < 1 µs, R_L = 12Ω		9		
D	Maximum Duty cycle		100			%
R_{BP}	Bypass Mode Resistance (Note 15)	$V_{IN} = V_{GS}$ = 3.1V, I_{OUT} = –500 mA VCON > 1.16V		75		mΩ
I_{OUT}	Maximum output current capability	2.7V ≤ V_{IN} ≤ 5.5V 2.5 × VCON ≤ V_{IN} – 285 mV	750			mA
		2.7V ≤ V_{IN} ≤ 5.5V 2.5 × VCON ≥ V_{IN} – 165 mV, Bypass mode	1000			
C_{VCON}	VCON input capacitance	VCON = 1V, Test frequency = 100 KHz		<1.0		pF
V_{OUT} Linearity	VCON range 0.16V to 1.44V	0mA ≤ I_{OUT} ≤ 750 mA (Note 14)	–3		+3	%
			–50		+50	mV
T_{ON}	Turn-on time (time for output to reach 95% final value after Enable low-to-high transition)	EN = Low-to-High V_{IN} = 4.2V, V_{OUT} = 3.4V I_{OUT} = < 1mA, C_{OUT} = 4.7 µF			50	µs
$T_{BP,\ NEG}$	Auto Bypass Detect Negative Threshold Delay Time	(Note 12)		10		µs
$T_{BP,\ POS}$	Auto Bypass Detect Positive Threshold Delay Time	(Note 13)		0.1		

Symbol	Parameter	Condition	Min	Typ	Max	Units
η	Efficiency	V_{IN} = 3.6V, V_{OUT} = 0.8V I_{OUT} = 10 mA, ECO mode		75		%
		V_{IN} = 3.6V, V_{OUT} = 1.8V I_{OUT} = 200 mA, PWM mode		90		
		V_{IN} = 3.9V, V_{OUT} = 3.3V I_{OUT} = 500 mA, PWM mode		95		
$LINE_{TR}$	Line transient response	V_{IN} = 3.6V to 4.2V, T_R = T_F = 10 µs, I_{OUT} = 100 mA, V_{OUT} = 0.8V		50		mVpk
$LOAD_{TR}$	Load transient response	V_{IN} = 3.1V/3.6V/4.5V, V_{OUT} = 0.8V, I_{OUT} = 50 mA to 150 mA T_R = T_F = 0.1 µs		50		mVpk

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pins.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 125°C (typ.).

Note 4: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200 pF capacitor discharged directly into each pin.

Note 5: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Note 6: Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7.

Note 7: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm. Due to the pulsed nature of the testing $T_A = T_J$ for the electrical characteristics table.

Note 8: The parameters in the electrical characteristics table are tested under open loop conditions at VIN = 3.6V unless otherwise specified. For performance over the input voltage range and closed-loop results, refer to the datasheet curves.

Note 9: Shutdown current includes leakage current of PFET.

Note 10: I_q specified here is when the part is not switching under test mode conditions. For operating quiescent current at no load, refer to datasheet curves.

Note 11: Current limit is built-in, fixed, and not adjustable.

Note 12: Entering Bypass Mode V_{IN} is compared to the programmed output voltage (2.5 × VCON). When V_{IN} – (2.5 × VCON) falls below $V_{BP,NEG}$ longer than $T_{BP,NEG}$, the Bypass FET turns on, and the switching FET turns on.

Note 13: Bypass Mode is exited when V_{IN} – (2.5 × VCON) exceeds $V_{BP,POS}$ longer than $T_{BP,POS}$, and PWM mode resumes. The hysteresis for the bypass detection threshold $V_{BP,POS}$-$V_{BP,NEG}$ will always be positive and will be approximately 50 mV.

Note 14: Linearity limits are ±3% or ±50 mV, whichever is larger. V_{OUT} is monotonic in nature with respect to VCON input.

Note 15: Total resistance in Bypass mode. Total includes the Bypass FET resistance in parallel with the PWM switch path resistance (PFET resistance and series inductor parasistic resistance.)

Note 16: All 0.4V V_{OUT} specifications are at steady-state only.

Note 17: FB has 200 kΩ to SGND.

Note 18: Care should be taken to keep the VCON pin voltage less than the VIN pin voltage as this can place the part into a manufacturing test mode.

Block Diagram

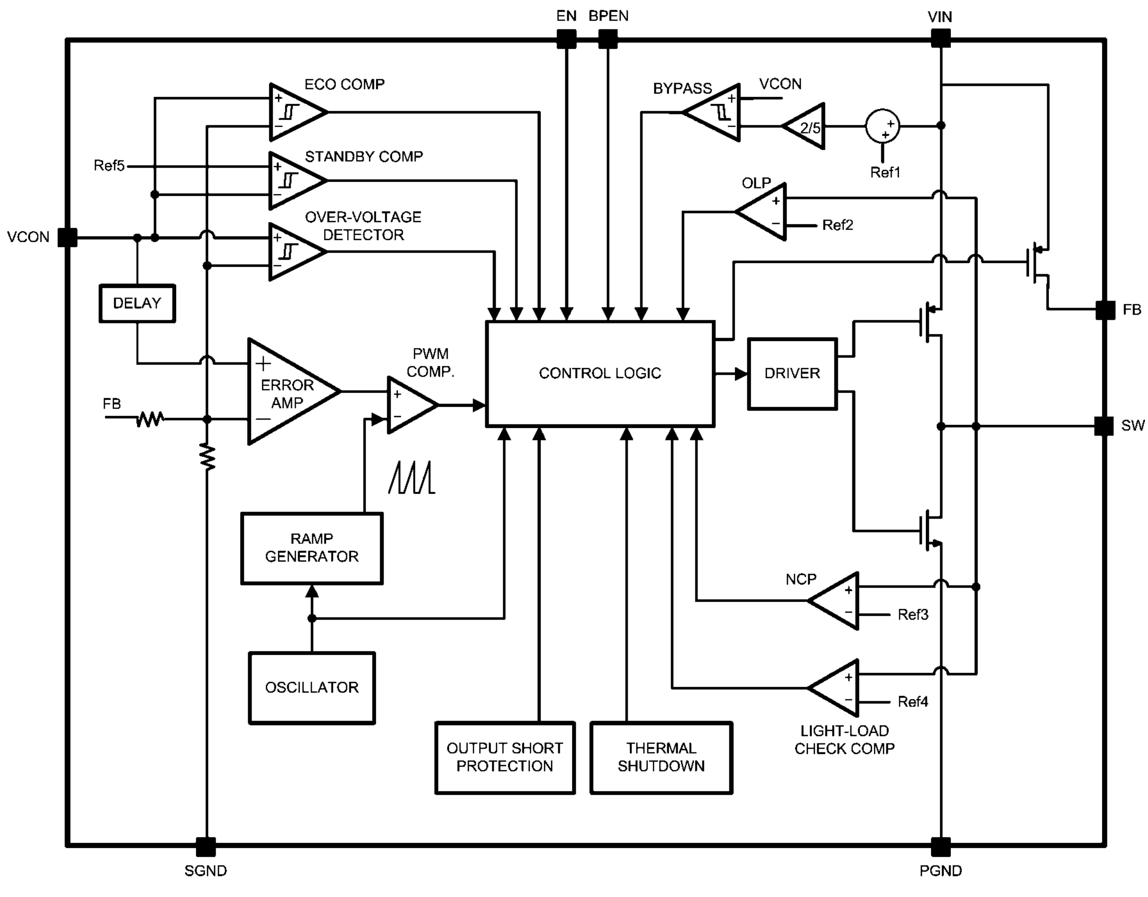
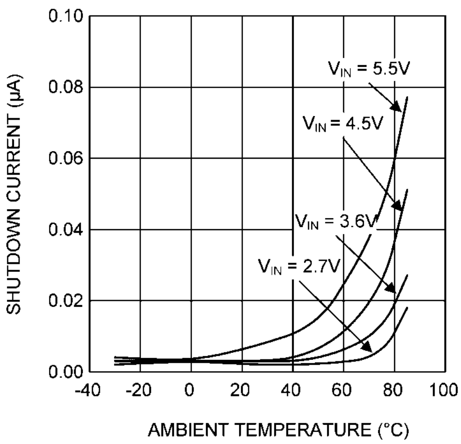


FIGURE 1. Functional Block Diagram

Typical Performance Characteristics

VIN = EN = 3.6V, L = 0.5 µH, C_{IN} = 10 µF, C_{OUT} = 4.7 µF and T_A = +25°C, unless otherwise noted.

Shutdown Current vs Temperature (SW=VCON=EN=0V)



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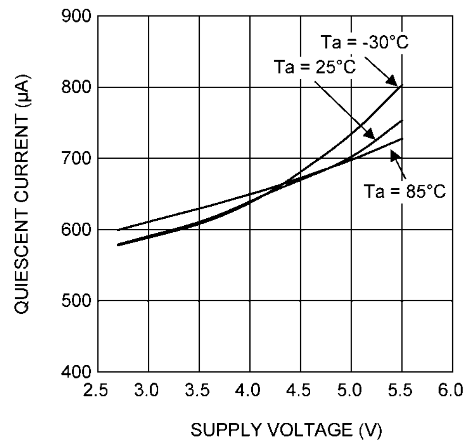
Quiescent Current vs Supply Voltage (No switching, FB=1V, VCON=0.13V)



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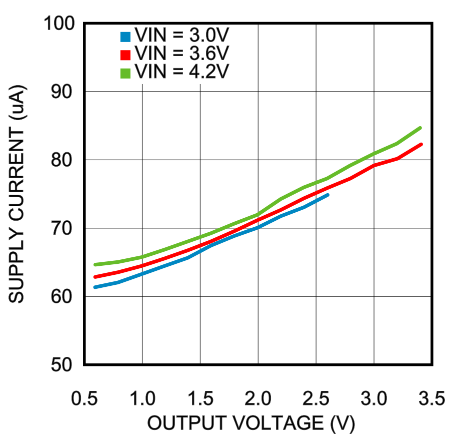
ECO mode Supply Current vs Output Voltage (Closed loop, Switching, No load)



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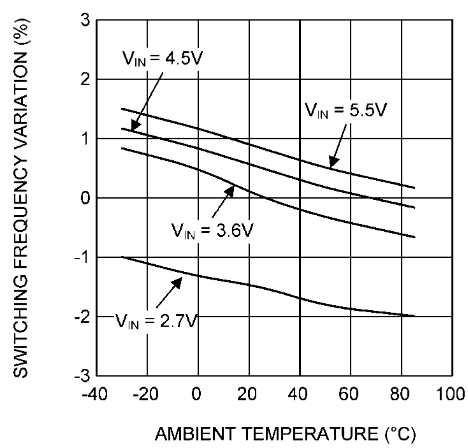
Switching Frequency vs Temperature (V_{OUT}= 2.0V, I_{OUT}=200 mA)



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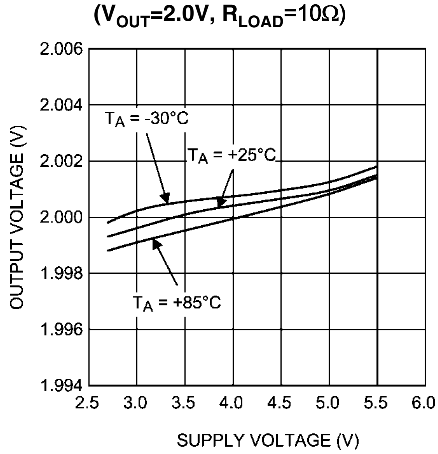
Output Voltage vs Supply Voltage (V_{OUT}=2.0V, R_{LOAD}=10Ω)



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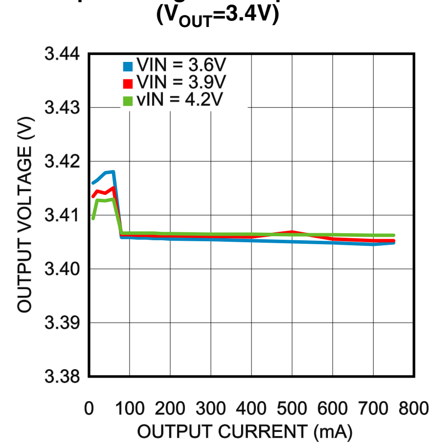
Output Voltage vs Output Current (V_{OUT}=3.4V)



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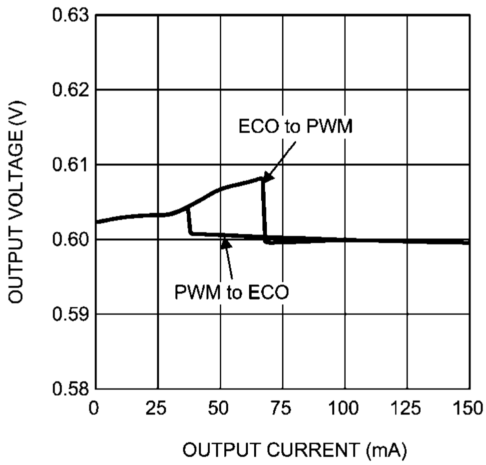
Output Voltage vs Output Current (V_{OUT}=0.6V)



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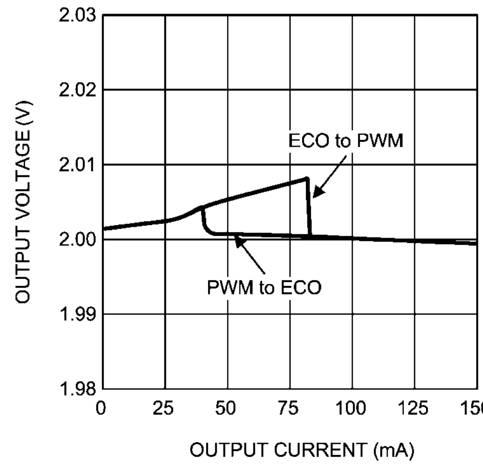
Output Voltage vs Output Current (V_{OUT}=2.0V)



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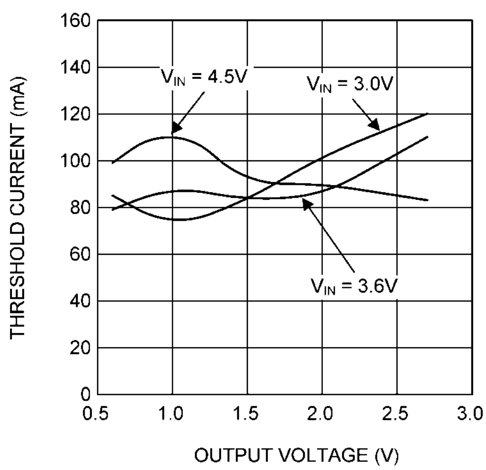
ECO-PWM mode Threshold Current vs Output Voltage



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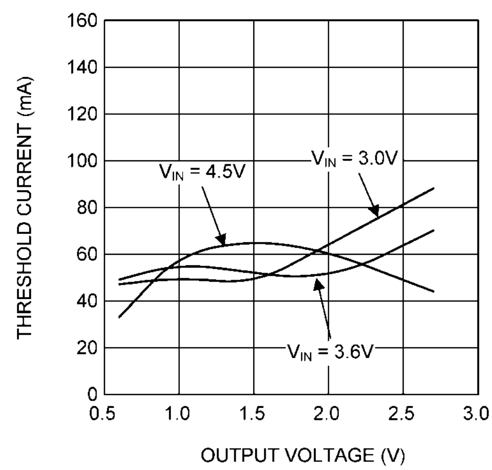
PWM-ECO mode Threshold current vs Output voltage



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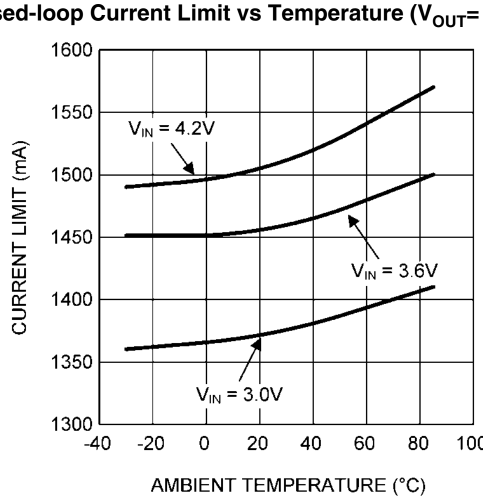
Closed-loop Current Limit vs Temperature (V_{OUT}= 2.0V)



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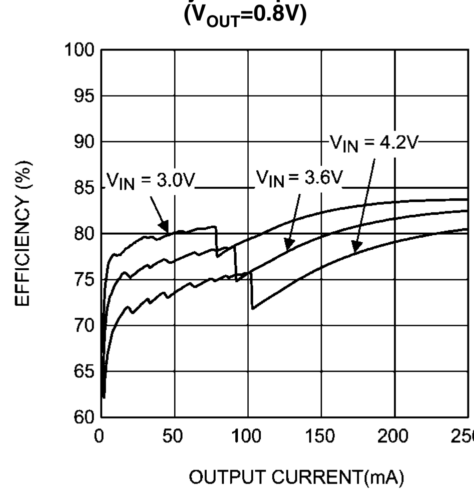
Efficiency vs Output Current (V_{OUT}=0.8V)



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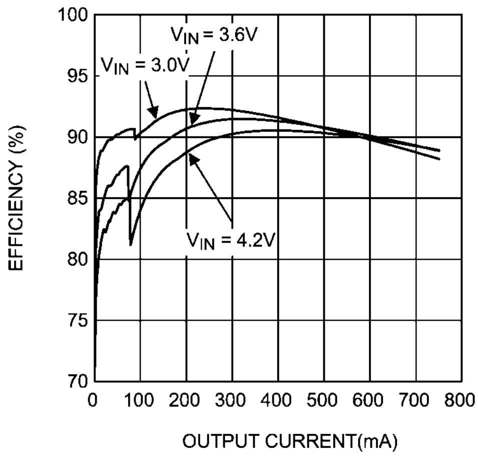
Efficiency vs Output Current (V_{OUT}=2.0V)



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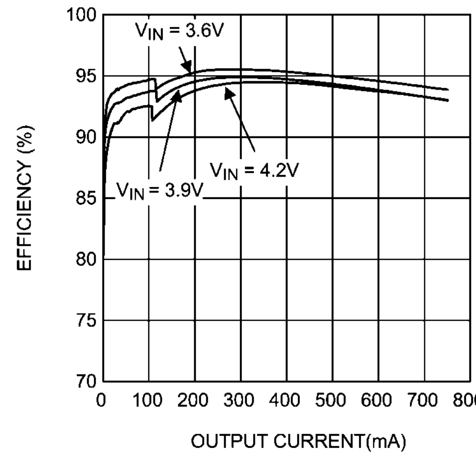
Efficiency vs Output Current (V_{OUT}=3.3V)



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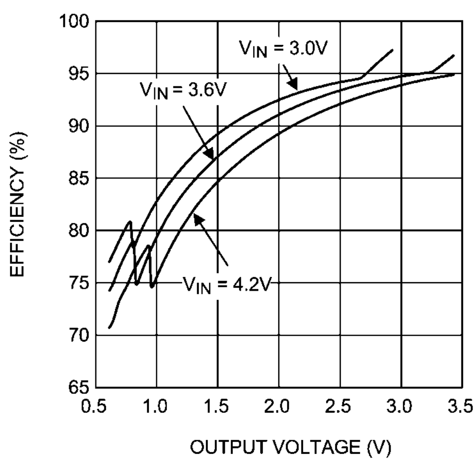
Efficiency vs Output Voltage (R_{LOAD}=10Ω)



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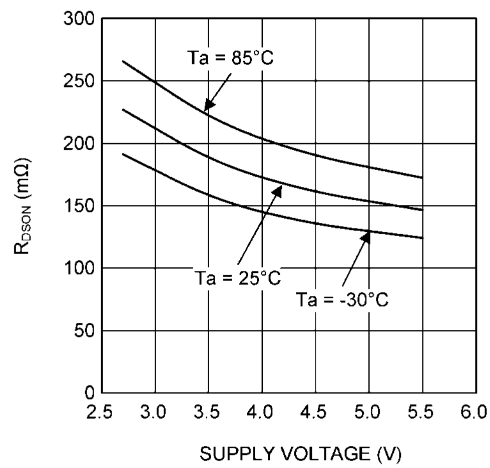
PFET R_{DSON} vs Supply Voltage



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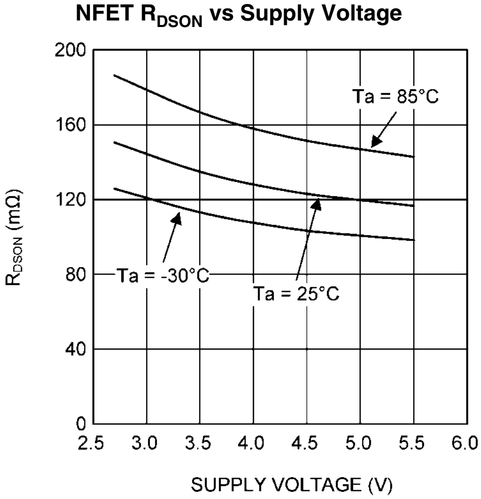
NFET R_{DSON} vs Supply Voltage



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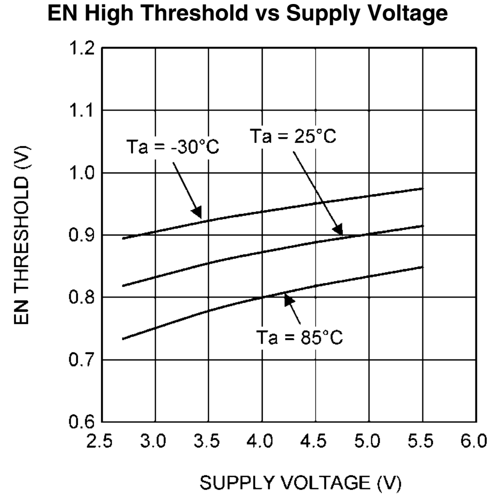
EN High Threshold vs Supply Voltage



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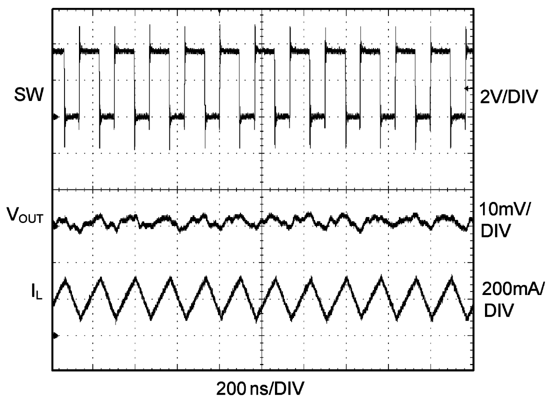
Output Voltage Ripple in PWM Mode
(V_{OUT}=2.0V, I_{OUT}=200 mA)



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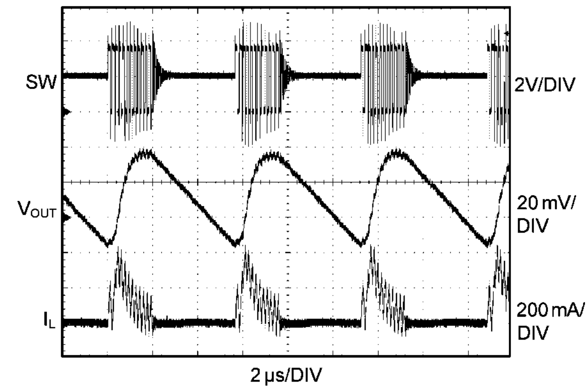
Output Voltage Ripple in ECO Mode
(V_{OUT}=2.0V, I_{OUT}=50 mA)



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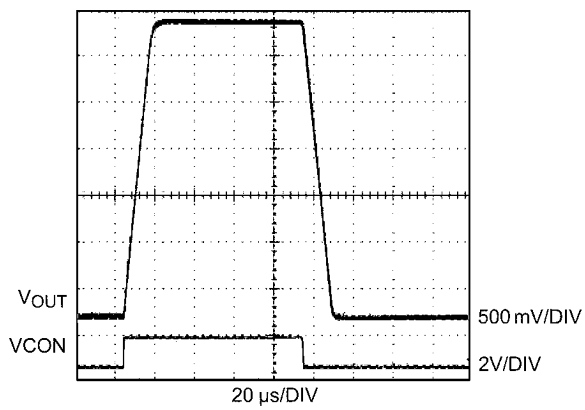
VCON Transient Response
(V_{IN}=3.9V, V_{OUT}=0.4V-3.6V, R_{LOAD}=10Ω)



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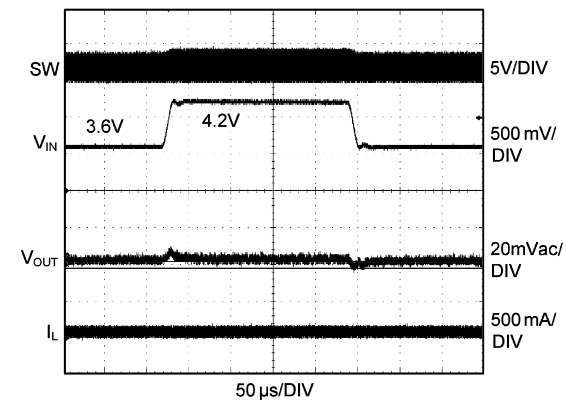
Line Transient Response
(V_{IN}=3.6V–4.2V, V_{OUT}=0.8V, R_{LOAD}=8Ω)



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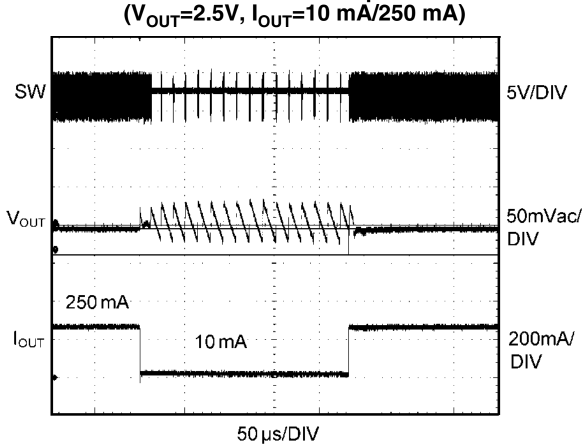
Load Transient Response
(V_{OUT}=2.5V, I_{OUT}=10 mA/250 mA)



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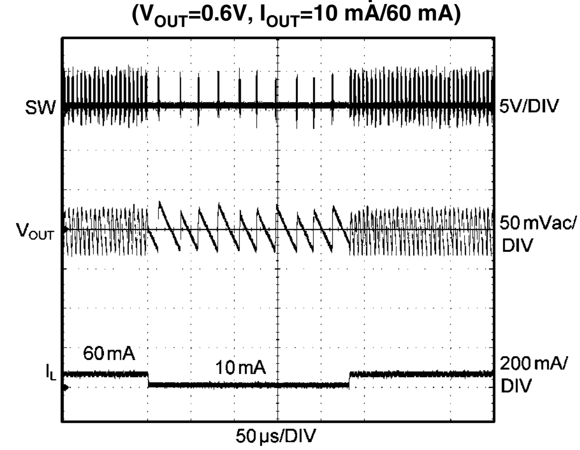
Load Transient Response
(V_{OUT}=0.6V, I_{OUT}=10 mA/60 mA)



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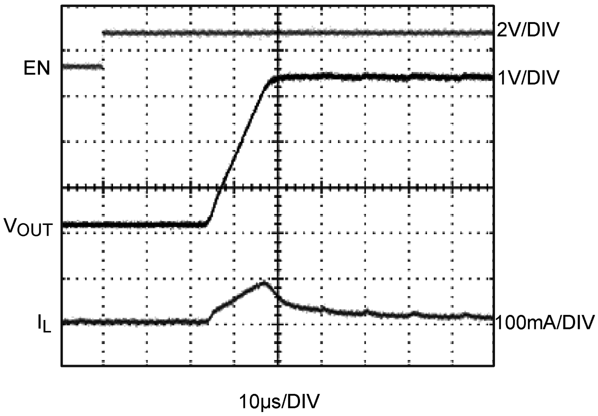
Startup
(V_{IN}=4.2V, V_{OUT}=3.4V, R_{LOAD}=3.6 KΩ)



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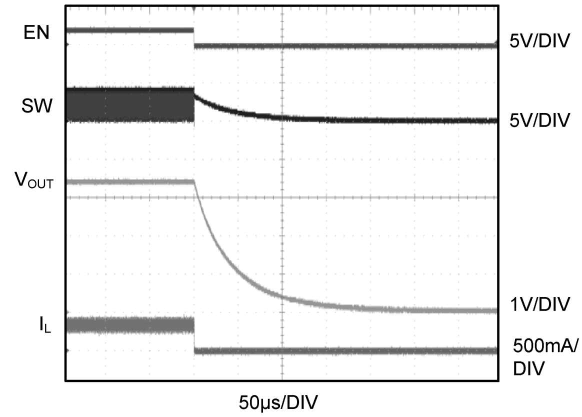
Shutdown
(V_{IN}=4.2V, V_{OUT}=3.4V, R_{LOAD}=10Ω)



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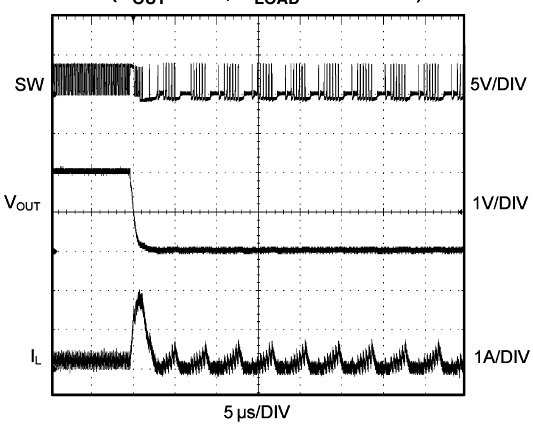
Timed Current Limit
(V_{OUT}=2.0V, R_{LOAD}=10Ω → 0Ω)



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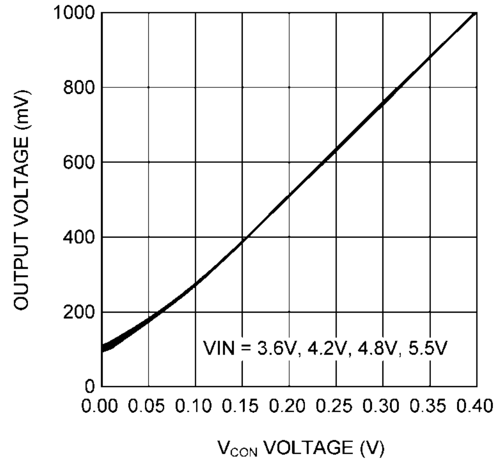
Low VCON Voltage vs Output Voltage (R_{LOAD}=10Ω)



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Operation Description

DEVICE INFORMATION

The LM3242 is a simple, step-down DC-DC converter optimized for powering RF power amplifiers (PAs) in mobile phones, portable communicators, and similar battery powered RF devices. It is designed to allow the RF PA to operate at maximum efficiency over a wide range of power levels from a single Li-Ion battery cell. It is based on a voltage-mode buck architecture, with synchronous rectification for high efficiency. It is designed for a maximum load capability of 750 mA in PWM mode. Maximum load range may vary from this depending on input voltage, output voltage and the inductor chosen.

There are five modes of operation depending on the current required: PWM (Pulse Width Modulation), ECO (ECOnomy), BP (Bypass), Sleep, and Shutdown. (See Table 1.) The LM3242 operates in PWM mode at higher load current conditions. Lighter loads cause the device to automatically switch into ECO mode. Shutdown mode turns the device off and reduces battery consumption to 0.1 µA (typ.).

DC PWM mode output voltage precision is ±2% for 3.6 V_{OUT}. Efficiency is typically around 95% (typ.) for a 500 mA load with 3.3V output, 3.9V input. The output voltage is dynamically programmable from 0.4V to 3.6V by adjusting the voltage on the control pin (VCON) without the need for external feedback resistors. This ensures longer battery life by being able to change the PA supply voltage dynamically depending on its transmitting power.

Additional features include current overload protection and thermal overload shutdown.

The LM3242 is constructed using a chip-scale 9-bump micro SMD package. This package offers the smallest possible size, for space-critical applications such as cell phones, where board area is an important design consideration. Use of a high switching frequency (6MHz, typ.) reduces the size of external components. As shown in the Typical Application Circuit, only three external power components are required for implementation. Use of a micro SMD package requires special design considerations for implementation. (See MICRO SMD PACKAGE ASSEMBLY AND USE section.) Its fine bump-pitch requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subject to high-intensity ambient red or infrared light. Also, the system controller should set EN low during power-up and other low supply voltage conditions. (See SHUTDOWN MODE below.)

CIRCUIT OPERATION

Referring to the Typical Application Circuit and Figure 1, the LM3242 operates as follows. During the first part of each switching cycle, the control block in the LM3242 turns on the internal top-side PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of around $(V_{IN} - V_{OUT}) / L$, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the bottom-side NFET synchronous rectifier on. In response, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope around V_{OUT} / L. The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at SW to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM MODE OPERATION

While in PWM mode operation, the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced. While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

BYPASS MODE OPERATION

The LM3242 contains an internal BPFET switch for bypassing the PWM DC-DC converter during Bypass mode. In Bypass mode, this BPFET is turned on to power the PA directly from the battery for maximum RF output power. When the part operates in the Bypass mode, the output voltage will be the input voltage less the voltage drop across the resistance of the BPFET in parallel with the PFET + Switch Inductor. Bypass mode is more efficient than operating in PWM mode at 100% duty cycle because the combined resistance is significantly less than the series resistance of the PWM PFET and inductor. This translates into higher voltage available on the output in Bypass mode, for a given battery voltage. The part can be set to bypass mode by sending BPEN pin high. This is called Forced Bypass Mode and it remains in bypass mode until BPEN pin goes low. Alternatively the part can go into Bypass mode automatically. This is called Auto-Bypass mode or Automatic Bypass mode. The bypass switch turns on when the difference between the input voltage and programmed output voltage is less than 200 mV (typ.) for longer than 10 µs (typ.). The bypass switch turns off when the input voltage is higher than the programmed output voltage by 250 mV (typ.) for longer than 0.1 µs (typ.). This method is very system resource friendly in that the Bypass PFET is turned on automatically when the input voltage gets close to the output voltage, a typical scenario of a discharging battery. It is also turned off automatically when the input voltage rises, a typical scenario when connecting a charger. When $V_{OUT} < 300$ mV, BPEN will be ignored.

ECO MODE OPERATION

At very light loads (50 mA to 100 mA), the LM3242 enters ECO mode operation with reduced switching frequency and supply current to maintain high efficiency. During ECO mode operation, the LM3242 positions the output voltage slightly higher (+7mV typ.) than the normal output voltage during PWM mode operation, allowing additional headroom for voltage drop during a load transient from light to heavy load.

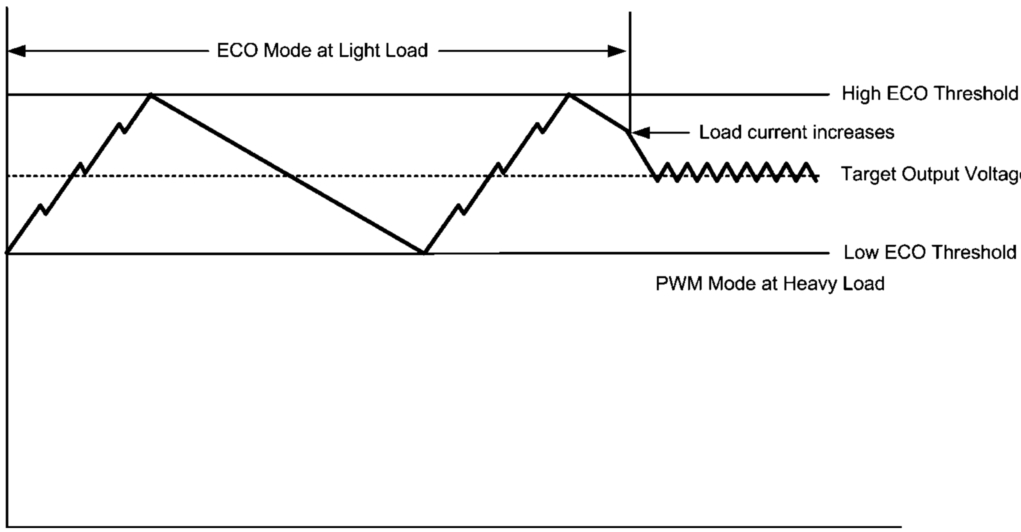

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FIGURE 2. Operation in ECO Mode and Transfer to PWM Mode

SLEEP MODE OPERATION

When VCON is less than 80 mV in 10 µs, the LM3242 will go into SLEEP mode — the SW pin will be in Tri-state (floating), which will operate like ECO mode with no switching. LM3242 will return to normal operation immediately when VCON ≥130 mV in PWM mode or ECO mode, depending on load detection.

SHUTDOWN MODE

Setting the EN digital pin low (<0.4V) places the LM3242 in Shutdown mode (0.1 µA typ.). During shutdown, the PFET switch, the NFET synchronous rectifier, reference voltage source, control and bias circuitry of the LM3242 are turned off. Setting EN high (>1.2V) enables normal operation. EN should be set low to turn off the LM3242 during power-up and under voltage conditions when the power supply is less than the 2.7V minimum operating voltage. The LM3242 has an UVLO (Under Voltage Lock Out) comparator to turn the power device off in the case the input voltage or battery voltage is too low. The typical UVLO threshold is around 2.0V for lock and 2.1V for release.

TABLE 1. Description of Modes

Mode	EN	BPEN	VCON	I_{OUT}
Shutdown	0	X	X	X
Sleep	1	0	< 80 mV	X
Pulse Width Modulation (PWM)	1	0	> 130 mV	> 100 mA
Economy (ECO)	1	0	< (V_{IN} – 0.2V)/2.5	< 50 mA
Bypass (BP)	1	0	> (V_{IN} – 0.2V)/2.5	X
	1	1	X	X

INTERNAL SYNCHRONOUS RECTIFICATION

While in PWM mode, the LM3242 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

With medium and heavy loads, the NFET synchronous rectifier is turned on during the inductor current down slope in the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

CURRENT LIMITING

The current limit feature allows the LM3242 to protect itself and external components during overload conditions. In PWM mode, the cycle-by-cycle current limit is a 1450 mA (typ.). If an excessive load pulls the output voltage down to less than 0.3V (typ.), the NFET synchronous rectifier is disabled and the current limit is reduced to 530 mA (typ.). Moreover, when the output voltage becomes less than 0.15V (typ.), the switching frequency will decrease to 3MHz, thereby preventing excess current and thermal stress.

DYNAMICALLY ADJUSTABLE OUTPUT VOLTAGE

The LM3242 features dynamically adjustable output voltage to eliminate the need for external feedback resistors. The output can be set from 0.4V to 3.6V by changing the voltage on the analog VCON pin. This feature is useful in PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances the transmitting power can be reduced. Hence the supply voltage to the PA can be reduced, promoting longer battery life. See *SETTING THE OUTPUT VOLTAGE* in the *Application Information* section for further details. The LM3242 moves into Pulse Skipping mode when duty cycle is over approximately 92% or less than approximately 15% and the output voltage ripple increases slightly.

THERMAL OVERLOAD PROTECTION

The LM3242 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. Both the PFET and the NFET are turned off. When the temperature drops below 125°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

SOFT START

The LM3242 has a soft-start circuit that limits in-rush current during startup. During startup the switch current limit is increased in steps. Soft start is activated if EN goes from low to high after VIN reaches 2.7V.

Application Information

SETTING THE OUTPUT VOLTAGE

The LM3242 features a pin-controlled adjustable output voltage to eliminate the need for external feedback resistors. It can be programmed for an output voltage from 0.4V to 3.6V by setting the voltage on the VCON pin, as in the following formula:

$$V_{OUT} = 2.5 \times VCON$$

When VCON is between 0.16V and 1.44V, the output voltage will follow proportionally by 2.5 times of VCON.

If VCON is less than 0.16V (V_{OUT} = 0.4V), the output voltage may not be well regulated. Refer to datasheet curve "Low VCON Voltage vs. Output Voltage" for details. This curve exhibits the characteristics of a typical part, and the performance cannot be guaranteed as there could be a part-to-part variation for output voltages less than 0.4V. For V_{OUT} lower than 0.4V, the converter might suffer from larger output ripple voltage and higher current limit operation.

FB

Typically the FB pin is connected to VOUT for regulating the output voltage maximum of 3.6V.

INDUCTOR SELECTION

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. Saturation current ratings are typically specified at 25°C so ratings over the ambient temperature of application should be requested from manufacturer.

Minimum value of inductance to guarantee good performance is 0.3 µH at bias current (I_{LIM} (typ.)) over the ambient temperature range. Shielded inductors radiate less noise and should be preferred. There are two methods to choose the inductor saturation current rating.

Method 1:

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as:

$$I_{SAT} > I_{OUT\_MAX} + I_{RIPPLE}$$

where

$$I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 \times L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f}\right)$$

- I_{RIPPLE}: average-to-peak inductor current
- I_{OUT_MAX}: maximum load current (750 mA)
- V_{IN}: maximum input voltage in application
- L minimum inductor value including worst-case tolerances (30% drop can be considered for Method 1)
- F: minimum switching frequency (5.7 MHz)
- V_{OUT}: output voltage

Method 2:

A more conservative and recommended approach is to choose an inductor that can handle the maximum current limit of 1600 mA.

The inductor's resistance should be less than around 0.1Ω for good efficiency. *Table 2* lists suggested inductors and suppliers.

TABLE 2. Suggested Inductors

Model	Size (W x L x H) (mm)	Vendor
MIPSZ2012D0R5	2.0 x 1.2 x 1.0	FDK
LQM21PNR54MG0	2.0 x 1.25 x 0.9	Murata
LQM2MPNR47NG0	2.0 x 1.6 x 0.9	Murata
CIG21LR47M	2.0 x 1.25 x 1.0	Samsung
CKP2012NR47M	2.0 x 1.25 x 1.0	Taiyo Yuden

CAPACITOR SELECTION

The LM3242 is designed for use with ceramic capacitors for its input and output filters. Use a 10 µF ceramic capacitor for input and a sum total of 4.7 µF ceramic capacitors for the output. They should maintain at least 50% capacitance at DC bias and temperature conditions. Ceramic capacitors types such as X5R, X7R, and B are recommended for both filters. These provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. *Table 3* lists some suggested part numbers and suppliers. DC bias characteristics of the capacitors must be considered when selecting the voltage rating and case size of the capacitor. If it is necessary to choose a 0603 (1608) size capacitor for V_{IN} and 0402 (1005) size capacitor for V_{OUT}, the operation of the LM3242 should be carefully evaluated on the system board. Use of a 2.2 µF capacitor in conjunction with multiple 0.47 µF or 1.0 µF capacitors in parallel may also be considered when connecting to power amplifier devices that require local decoupling.

TABLE 3. Suggested Capacitors and Their Suppliers

Capacitance	Model	Size (Wx L) (mm)	Vendor
2.2 µF	GRM155R60J225M	1.0 x 0.5	Murata
2.2 µF	C1005X5R0J225M	1.0 x 0.5	TDK
2.2 µF	CL05A225MQ5NSNC	1.0 x 0.5	Samsung
4.7 µF	C1608JB0J475M	1.6 x 0.8	TDK
4.7 µF	C1005X5R0J475M	1.0 x 0.5	TDK
4.7 µF	CL05A475MQ5NRNC	1.0 x 0.5	Samsung
10 µF	C1608X5R0J106M	1.6 x 0.8	TDK
10 µF	GRM155R60J106M	1.0 x 0.5	Murata
10 µF	CL05A106MQ5NUNC	1.0 x 0.5	Samsung

The input filter capacitor supplies AC current drawn by the PFET switch of the LM3242 in the first part of each cycle and reduces the voltage ripple imposed on the input power source. The output filter capacitor absorbs the AC inductor current, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR (Equivalent Series Resistance) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple.

MICRO SMD PACKAGE ASSEMBLY AND USE

Use of the micro SMD package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in Texas Instruments Application Note 1112. Refer to the section *Surface Mount Technology (SMD) Assembly Considerations.* For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with micro SMD package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See Application Note 1112 for specific instructions how to do this.

The 9-bump package used for LM3242 has 250 micron solder balls and requires 0.225 mm pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90°angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 7mil wide, for a section approximately 7mil long, as a thermal relief. Then each trace should neck up or down to its optimal width. The important criterion is symmetry. This ensures the solder bumps on the LM3242 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A3 and C3. Because VIN and GND are typically connected to large copper planes, inadequate thermal reliefs can result in late or inadequate re-flow of these bumps.

The micro SMD package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the micro SMD package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, micro SMD devices are sensitive to light, in the red and infrared range, shining on the package's exposed die edges.

It is recommended to add a 10 nF capacitor between VCON and ground for non-standard ESD events or environments and manufacturing processes. It prevents unexpected output voltage drift.

PCB Board Layout Considerations

OVERVIEW

PC board layout is critical to successfully designing a DC-DC converter into a product. As much as a 20 dB improvement in RX noise floor can be achieved by carefully following recommended layout practices. A properly planned board layout optimizes the performance of a DC-DC converter and minimizes effects on surrounding circuitry while also addressing manufacturing issues that can have adverse impacts on board quality and final product yield.

PCB CONSIDERATIONS

Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. Erroneous signals could be sent to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the micro SMD package and board pads. Poor solder joints can result in erratic or degraded performance of the converter.

ENERGY EFFICIENCY

Minimize resistive losses by using wide traces between the power components and doubling up traces on multiple layers when possible.

EMI

By its very nature, any switching converter generates electrical noise, and the circuit board designer's challenge is to minimize, contain, or attenuate such switcher-generated noise. A high-frequency switching converter, such as the LM3242, switches Ampere level currents within nanoseconds, and the traces interconnecting the associated components can act as radiating antennas. The following guidelines are offered to help to ensure that EMI is maintained within tolerable levels.

To minimize radiated noise:

- Place the LM3242 switcher, its input capacitor, and output filter inductor and capacitor close together, and make the interconnecting traces as short as possible.
- Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the internal PFET of the LM3242 and the inductor, to the output filter capacitor, then back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the internal synchronous NFET of the LM3242 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
- Make the current loop area(s) as small as possible.

To minimize ground-plane noise:

- Reduce the amount of switching current that circulates through the ground plane: Connect the ground bumps of the LM3242 and its input filter capacitor together using generous component-side copper fill as a pseudo-ground plane. Then connect this copper fill to the system ground-plane (if one is used) with multiple vias. These multiple vias help to minimize ground bounce at the LM3242 by giving it a low-impedance ground connection.

To minimize coupling to the DC-DC converter's own voltage feedback trace:

- Route noise sensitive traces, such as the voltage feedback path, as directly as possible from the switcher FB pad to the VOUT pad of the output capacitor, but keep it away from noisy traces between the power components.

To decouple common power supply lines, series impedances may be used to strategically isolate circuits:

- Take advantage of the inherent inductance of circuit traces to reduce coupling among function blocks, by way of the power supply traces.
- Use star connection for separately routing VBATT to PVIN and VBATT_PA.
- Inserting a single ferrite bead in-line with a power supply trace may offer a favorable tradeoff in terms of board area, by allowing the use of fewer bypass capacitors.

MANUFACTURING CONSIDERATIONS

The LM3242 package employs a 9-bump (3x3) array of 250 micron solder balls, with a 0.4mm pad pitch. A few simple design rules will go a long way to ensuring a good layout.

- Pad size should be 0.225 ± 0.02 mm. Solder mask opening should be 0.325 ± 0.02 mm.
- As a thermal relief, connect to each pad with 7 mil wide, 7 mil long traces, and incrementally increase each trace to its optimal width. Symmetry is important to ensure the solder bumps re-flow evenly (refer to TI Application Note AN-1112 MicroSMD Wafer Level Chip Scale Package).

LM3242 EVALUATION BOARD

The following figures are drawn from a 4-layer board design, with notes added to highlight specific details of the DC-DC switching converter section.

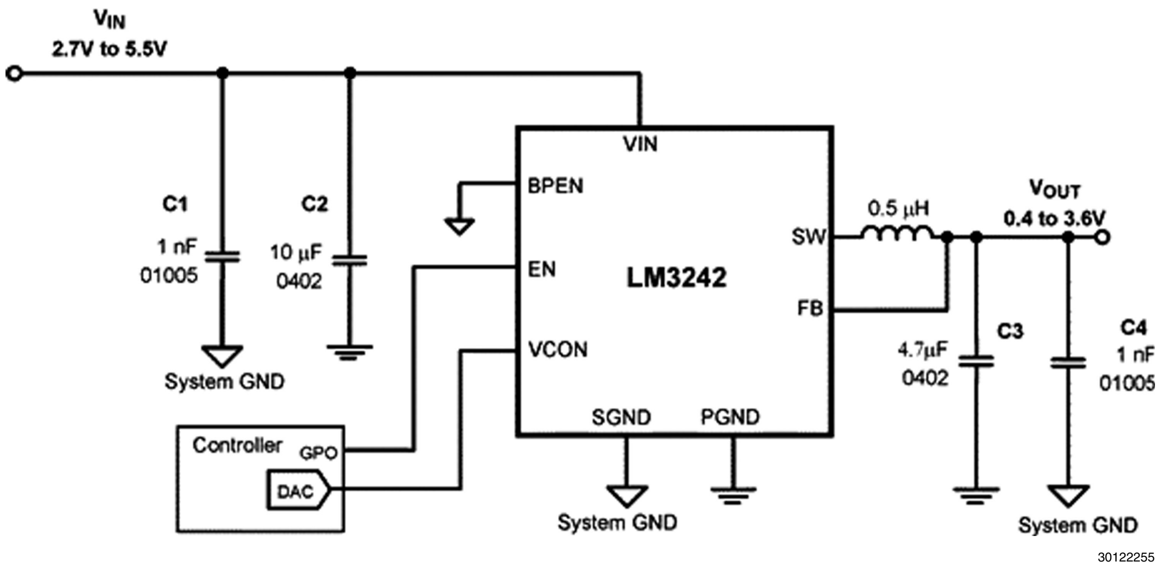


FIGURE 3. Simplified LM3242 RF Evaluation Board Schematic

1. Bulk Input Capacitor C2 should be placed closer to LM3242 than C1.
2. Add a 1nF (C1) on input of LM3242 for high frequency filtering.
3. Bulk Output Capacitor C3 should be placed closer to LM3242 than C4.
4. Add a 1nF (C4) on output of LM3242 for high frequency filtering.
5. Connect both GND terminals of C1 and C4 directly to System GND layer of phone board.
6. Connect bumps SGND (A2), NC (B2), BPEN (C1) directly to System GND.
7. Use 0402 caps for both C2 and C3 due to better high frequency filtering characteristics over 0603 capacitors.
8. TI has seen some improvement in high frequency filtering for small bypass caps (C1 and C4) when they are connected to System GND instead of same ground as PGND. These capacitors should be 01005 case size for minimum footprint and best high frequency characteristics.

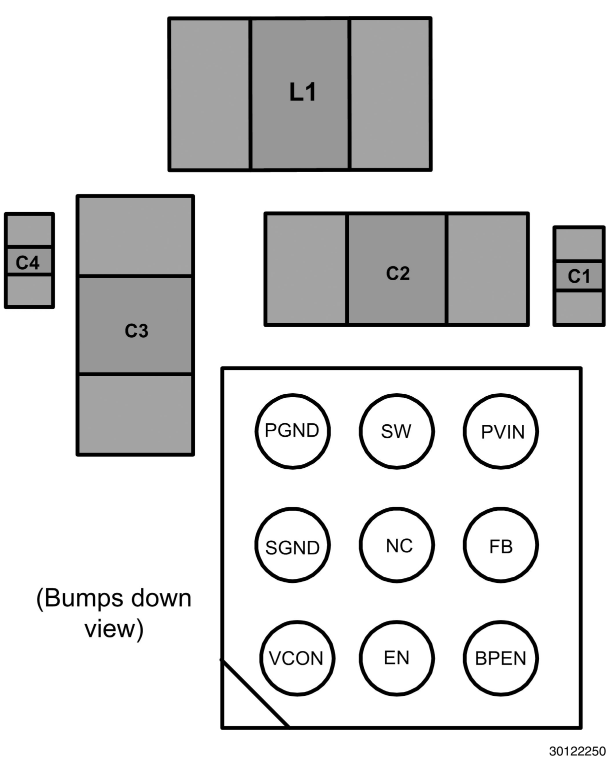


FIGURE 4. LM3242 Recommended Parts Placement (Top View)

Component Placement

- PVIN
  1. Use a star connection from PVIN to LM3242 and PVIN to PA VBATT connection (V_{CC1}). Do not daisy-chain PVIN connection to LM3242 circuit and then to PA device PVIN connection.
- TOP LAYER
  1. Place a via in LM3242 SGND(A2), BPEN(C1) pads to drop and connect directly to System GND Layer 4.
  2. Place two vias at LM3242 SW solder bump to drop VSW trace to Layer 3.
  3. Connect C2 and C3 capacitor GND pads to PGND bump on LM3242 using a star connection. Place vias in C2 and C3 GND pads that connect directly to System GND Layer 4.
  4. Add 01005/0201 capacitor footprints (C1,C4) to input/output of LM3242 for improved high frequency filtering. C1 and C4 GND pads connect directly to System GND Layer 4.
  5. Place three vias at L1 inductor pad to bring up VSW trace from Layer 3 to top Layer.
- LAYER 2
  1. Make FB trace at least 10 mils (0.254 mm) wide.
  2. Isolate FB trace away from noisy nodes and connect directly to C3 output capacitor. Place a via in LM3242 SGND(A2), BPEN(C1) pads to drop and connect directly to System GND Layer 4.
- LAYER 3
  1. Make VSW trace at least 15 mils (0.381mm) wide.
- LAYER 4 (System GND
  1. Connect C2 and C3 PGND vias to this layer.
  2. Connect C1 and C4 GND vias to this layer.
  3. Connect LM3242 SGND(A2), BPEN(C1), NC(B2) pad vias to this layer.

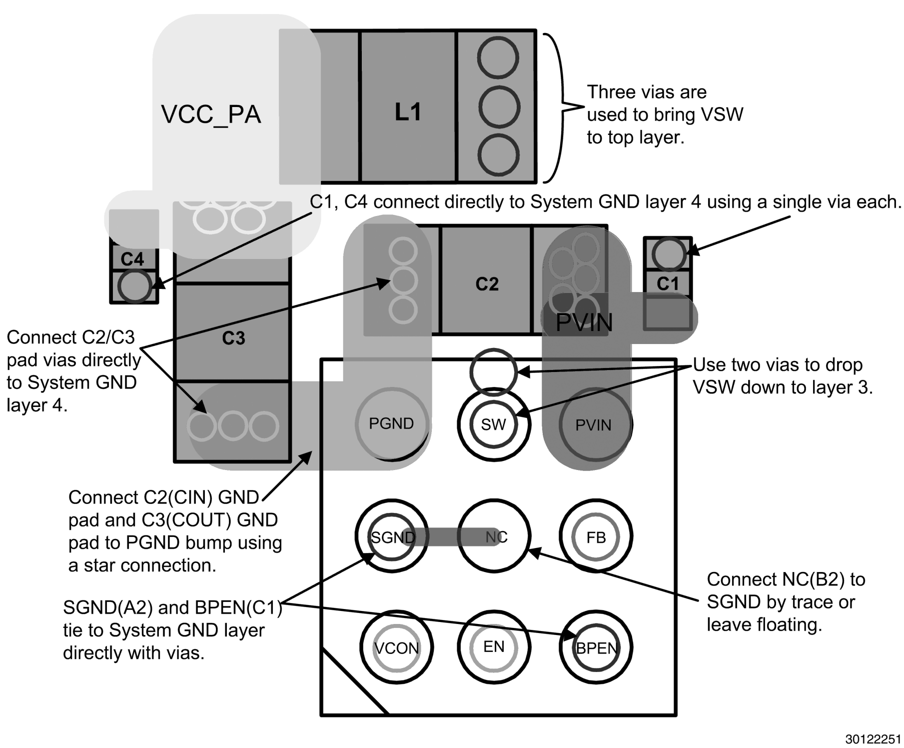


FIGURE 5. Board Layer 1 – PVIN and PGND Routing

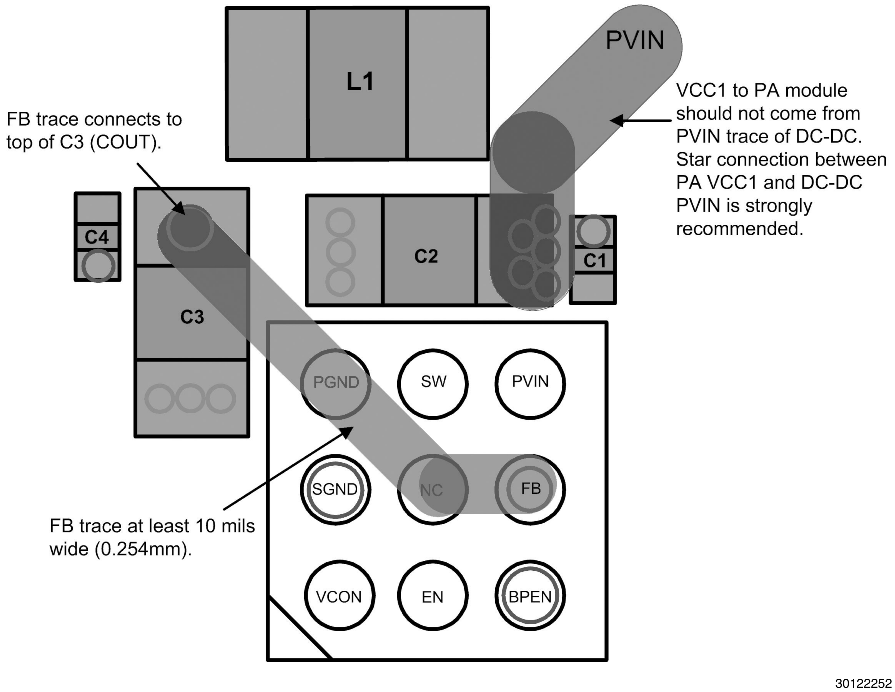


FIGURE 6. Board Layer 2 – FB and PVIN Routing

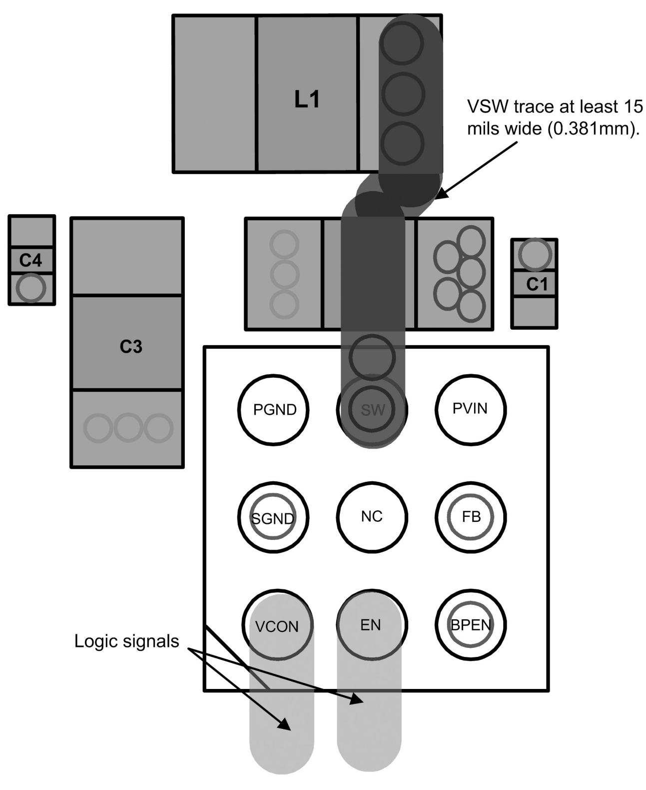


FIGURE 7. Board Layer 3 – SW, VCON and EN Routing

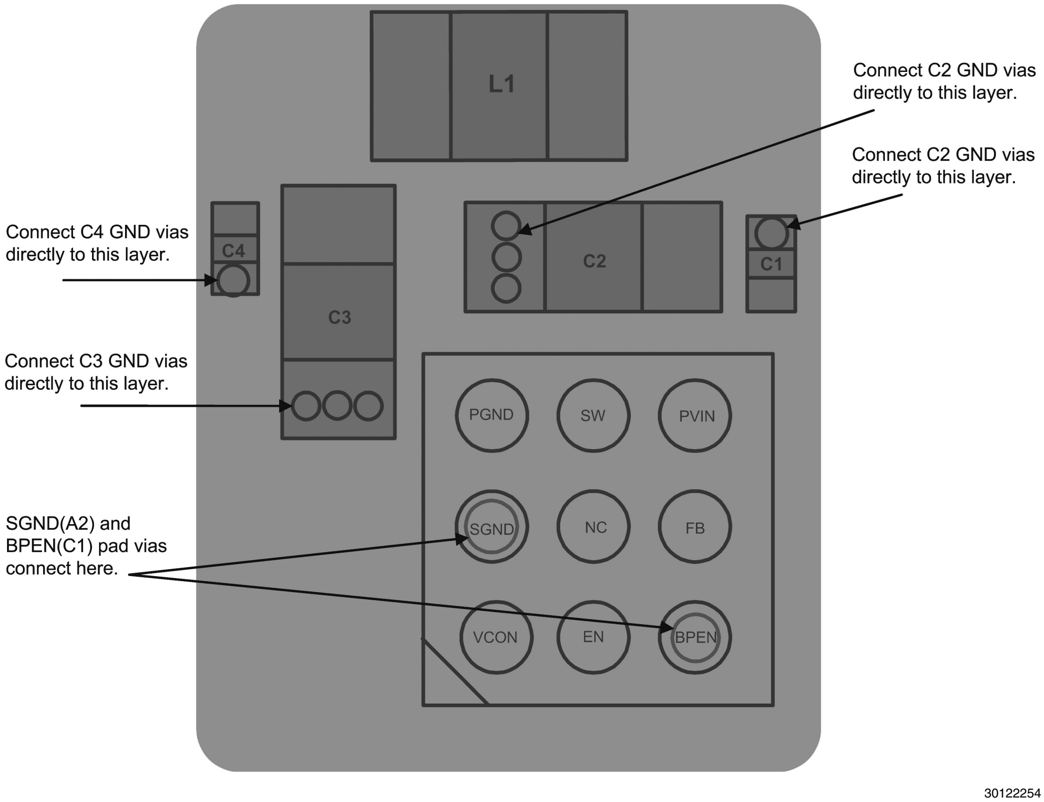
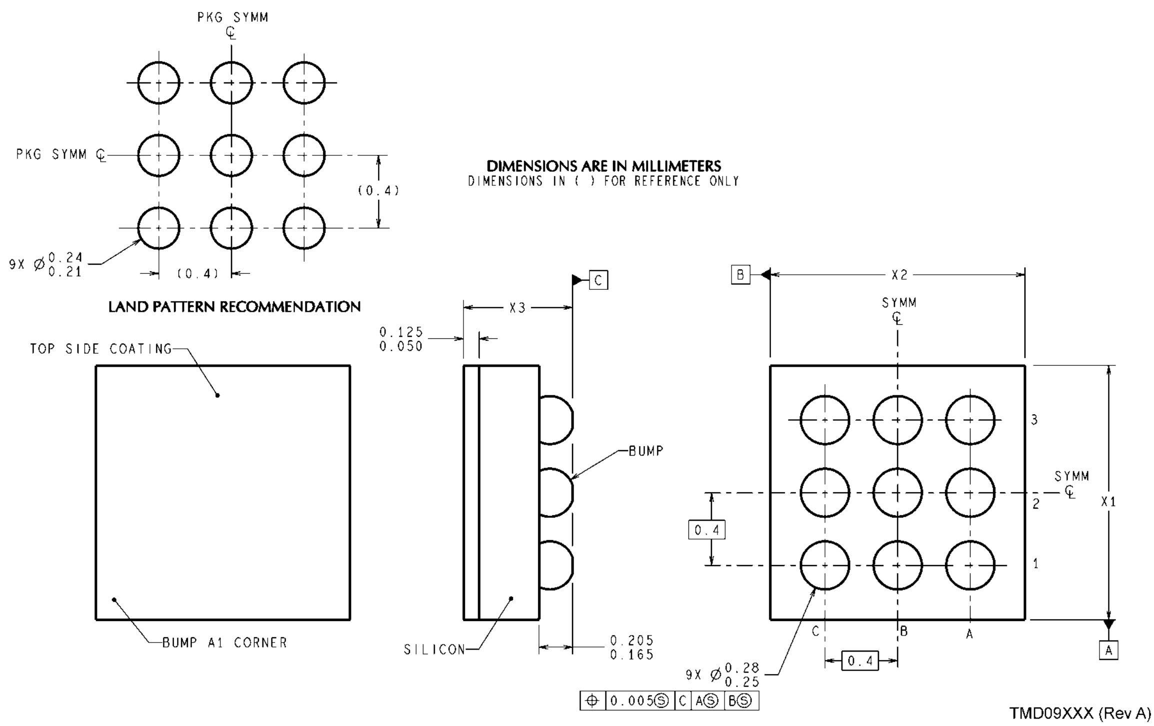


FIGURE 8. Board Layer 4 – System GND Plane

Physical Dimensions inches (millimeters) unless otherwise noted



TMD09XXX (Rev A)

9-Bump Thin Micro SMD, Large Bump (0.4 mm pitch)
NS Package Number TMD09
X1 = 1.35 mm ±0.030 mm
X2 = 1.488 mm ±0.030 mm
X3 = 0.6 mm ±0.075 mm

Notes

Notes

IMPORTANT NOTICE

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
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